THE 64TH SYMPOSIUM ON SEMICONDUCTORS
AND INTEGRATED CIRCUITS TECHNOLOGY

ADVANCED PROGRAM

◇ Thursday, June 5 ◇ 9:45〜17:00

<9:45>
Opening remarks by Symposium Chair
S.Oda Tokyo Institute of Technology

<9:50>
The 63rd SSICT Award

<10:00〜10:50>
1. Mechanism of mobility reduction for MISFET with high-k gate dielectrics
S.Saito Hitachi Ltd. (invited)

<10:50〜11:15>
2. Electrical properties of HfO_2 films prepared by remote plasma oxidation of Hf metal
K.Yanamoto, S.Hayashi, Y.Harada, M.Kubota, M. Niwa, M.Asai*, S.Horii *
. Matsushita Electric Industrial, Hitachi Kokusai Electric*

<11:15〜12:05>
3. Scaling Hf-based high-k gate stacks to(sub)1.0nm EOT : a status update.
Stefan de Gendt IMEC (invited)

<12:05〜13:00> Lunch

<13:00〜13:50>
4. The emerging new memories: their characteristics and application
Hongsik Jeong Samsung Electronics(invited)

<13:50〜14:15>
5. Non-volatile logic with ferroelectric technology
T.Nakamura, Y.Fujimori, H.Takasu Rohm

<14:15〜14:40>
6. Preparation and characterization of ferroelectric $BiFeO_3$ thin films.
KY. Yun, M.Noda, M.Okuyama Osaka Univ.

<14:40〜15:05>
7. Flash CVD technology
H.Yamoto, M.Shoji, K.Akuto, H.Kobayashi, H.Watanuki, K.Nagaoka, M.Fukagawa, R. Sakai Wacom Electric

<15:05〜15:20> Break

<15:20〜16:10>
8. MONOS nonvolatile semiconductor memory technology
S.Minami Renesas Technology Corp. (invited)

<16:10〜16:35>
9. ESR study of silicon nitride film used in MONOS nonvolatile semiconductor memory
Y.Shishido, Y.Kamigaki, I.Fujiwara*
Kagawa Univ., Sony Corp*

<16:35〜17:00>
10. Thick oxide layer fabrication process for silicon RF ICs
K.Tsuruta,T.Shibata Denso Corp.

<17:00〜18:00> — Banquet —

◇ Friday, June 6 ◇ 9:30〜16:40

<9:30〜10:20>
11. Present stage of 65nm-node low-k materials and processes
K.Nobuyoshi
Semiconductor Leading Edge Technologies (invited)

<10:20〜10:45>
12. Molecular design and syntheses of ultra tough organic low-k dielectrics
N.Aoi,T.Fukuda,H.Yanazawa ASET

<10:45〜11:10>
13. Low dielectric porous diamond film composed of diamond nano-particles
H.Sakaue, H.Tomimoto*, S.Ishikawa**, S.Shingubara, T.Takahagi Hiroshima Univ, JST*,Daiken Chemical**

<11:10〜12:00>
14. Stress engineering of multi-level interconection module with copper and low-k dielectric
M. Hasunuma Toshiba (invited)

<12:00〜13:00> Lunch

<13:00〜13:50>
15. ULSI Interconnection formaed by electroless Cu plating without Pd catalysis
S.Shingubara Hiroshima Univ. (invited)

<13:50〜14:15>
16. WIWNU improvement of electrochemical Cu plating on thin seed layer
H.suzuki, K.Nomura, K.Ide, H.Kanda, K.Mishima
Ebara Corp.

<14:15〜15:05>
17. Correlation between microstructure and reliability of Cu interconnects.
M.Moriyama Kyoto Univ. (invited)

<15:05〜15:20> Break

<15:20〜15:45>
18. Growth of Cu and Ta films by metal chloride reduction CVD
H.Sakamoto, Y.Ogura, Y.Ooba, N.Yahata
Mitsubishi Heavy Industries

<15:45〜16:10>
19. Reliability improvement of 90nm-node Cu / low - k interconnect
K.Hashimoto, SMatsumoto*, A.Ishii, K.Tomita,Y.Nishioka, M.Sekiguchi*,A.Iwasaki**, S.Isono*,T.Satake*, G.Okazaki*, M.Fujisawa, M.Matsumoto,S.Yamamoto,M.Matsuura
Renesas Technology Corp.,
*Matsushita Electric Industrial CO., Ltd.
**Matsushita Semi-Conductor Engineering Co., Ltd.

<16:10〜16:35>
20. Reliability in copper interconnects with SiLK interlevel dielectrics
M.Sato,H.Mori*,Y.Matsuoka,H,Matsuyama*,K.Shono*
Fujitsu VLSI Ltd., Fujitsu Ltd.*

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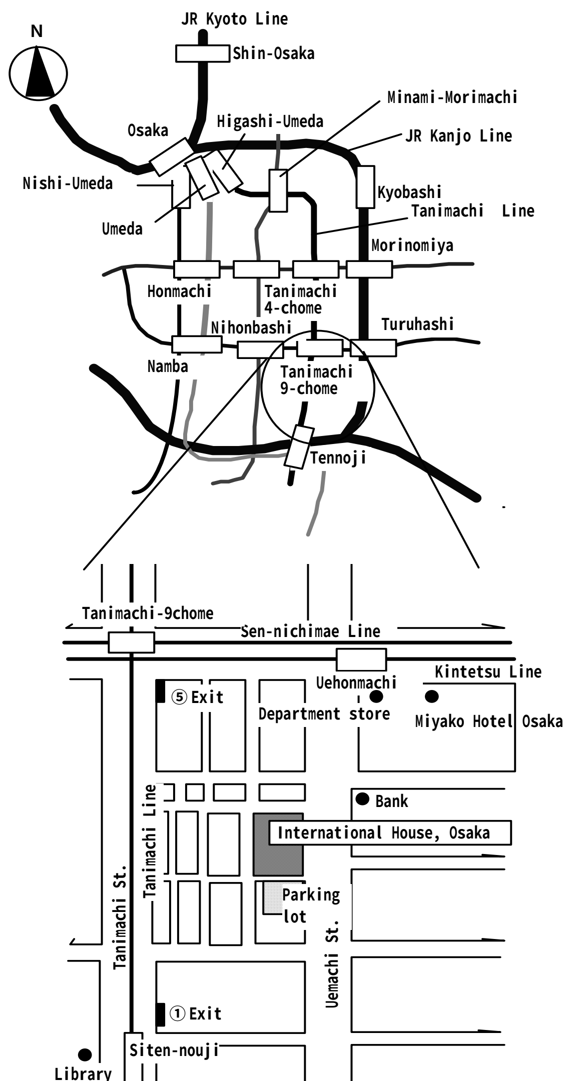

Traffic:
- 10 minutes walk from Tanimachi 9-chome Station (Tanimachi & Sennichimae Lines)
- 5 minutes walk from Uehonmachi Station(Kintetsu Line)

Symposium Chair; Shunri Oda, (*Tokyo Institute of Technology*),
Program Chair; Masafumi Kubota(*Matsushita Electric*)
Co-chair: Kiyoteru Kobayashi(*Renesas Technology*)

Electronic Materials Committee

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THE 64TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

International House, Osaka,Japan June 5-6, 2003

Organized by:
Electronic Materials Committee,
The Electrochemical Society of Japan.

The 64th Symposium on Semiconductors and Integrated Circuits Technology will be held on June 5-6, 2003 in Osaka, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on interconnect technology and advanced process/device technology for deep sub-micron regime.