THE 66TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

ADVANCED PROGRAM

◇ Thursday, **June 24** ◇ 9:55～16:50

<9:55～10:00> Opening remarks by symposium chair

<10:00～10:40>
1. Cu damascene process: status and challenges in electrochemical aspects.
H. Akaboshi, Hitachi. **(Invited)**

<10:40～11:20>
2. Photo-enhanced electrochemical mechanical polishing for Cu damascene
H. Yano, Toshiba. **(Invited)**

<11:20～11:45>
3. High reliability Cu interconnection utilizing a low contamination CoWP capping layer
T. shigami, T. Kurokawa, Y. Kakuhara, M. Sekine and K. Ueno, NEC Electronics.

<11:45～12:10>
4. Formation of diffusion barrier layer for ULSI Cu interconnection using a wet process.
M. Yoshino, T. Yokoshima, T. Masuda, J. Sasano, I. Matsuda, and T. Osaka, Waseda University.

<12:10～13:00> Lunch

<13:00～13:40>
5. Evaluation of wafer back grinding damage using photo luminescence
M. Watanabe, SEZ Japan. **(Invited)**

<13:40～14:20>
6. Ultra-high-density packaging by three-dimensional system integration
K. Takahashi, ASET. **(Invited)**

<14:20～15:00>
7. Highly reliable Cu/Low-k dual damascene interconnect technology for 65nm node
F. Ito, M. Ueki, M. Narihiro, H. Ohtake, M. Tagami, M. Tada, M. Abe, N. Inoue, K. Arai, T. Takeuchi, S. Saito, T. Onodera, N. Furutake, M. Hiroi, M. Sekine, and Y. Hayashi
NEC. **(Invited)**

<15:00～15:20> Break

<15:20～15:45>
8. Properties of a tantalum nitride source Ta(N-t-C5H11)[N(CH3)2]3 for MOCVD
S. Yasuhara, Y. Okuhara, and H. Kadokura, Kojundo Chemical Laboratory

<15:45～16:10>
9. A noble process for multilevel interconnects with effective reduction of PFC etching gases and energy consumption and high cost performance：line－pillar process
H. Itoh, K. Shimokawa, S. Sekiyama, and H. Yanazawa, ASET.

<16:10～16:50>
10. Integration of Cu/low-k dual-damascene interconnects with a porous PAE/SiOC hybrid structure for 65nm-node high performance eDRAM
R. Kanamura, Y.Ohoka, M. Fukasawa, K. Tabuchi, K. Nagahata, S. Shibuki, M. Muramatsu, H. Miyajima*, T. Usui*, A. Kajita*, K. Honda*, H. Shibata*, and S. Kadomura,
Sony, Toshiba*. **(Invited)**

<17票)3 3」S 0>0>SSICT Award

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◇ Friday , **June 25** ◇ 9:40～16:45

<9:40～10:30>
11. Recent progress in FET-type ferroelectric memories
H. Ishiwara, Tokyo Institute of Technology. **(Invited)**

<10:30～10:55>
12. 0.18μm FeRAM embedded system LSI
T. Ito, Y. Nagano, T. Mikawa, T. Kutsunai, S. Natsume, T. Tatsunari, K. Ohta, A. Noma, and Y. Judai, Matsushita.

<10:55～11:05> Break

<11:05～11:55>
13. Expectation for MRAM and current status of its development towards the realization of non-volatile solid-state RAM
S. Ikegawa[1], N Ishiwata[2], S. Tahara[2], and H. Yoda[1],
[1]Toshiba, [2]NEC. **(Invited)**

<11:55～12:20>
14. Novel sputtering technology of magnetic tunnel junctions for MRAM application
D. D. Djayaprawira, K. Tsunekawa, H. Maehara, M. Nagai, Y. Nagamine, and N. Watanabe, ANELVA.

<12:20～13:10> Lunch

<13:10～13:50>
15. Future trend of NAND flash technology
R. Shirota, Toshiba. **(Invited)**

<13:50～14:30>
16. AG-AND type flash memory enabling high data -throughput with multi-level programming.
Y. Sasago, Hitachi. **(Invited)**

<14:30～14:55>
17. 90nm NOR flash process integration technology for 90nm generation and beyond.
S. Yamagata, K. Hirohama, T. Takeuchi, T. Doi, T. Sonoda, N. Matsumoto, H. Komeda, H. Inuzuka, A. Nakamura, T. Harazono, K. Nakamura, K. Hironaka, N. Takeuchi, and S. Sato, Sharp.

<14:55～15:05> Break

<15:05～15:30>
18. Ultra-High speed direct tunneling memory (DTM) for system LSI.
K. Tsunoda, H. Tashiro, A. Sato, K. Ohira, T. Nakanishi, H. Tanaka, and Y. Arimoto, Fujitsu.

<15:30～15:55>
19. Single electron memory devices based on nanocrystalline silicon dots.
S. Y. Huang, S. Oda, Tokyo Institute of Technology.

<15:55～16:45>
20. Phase-change electronic memory: Ovonic unified memory (OUM) and cognitive computer device development at ECD/OVONYX
T. Ohta, Energy Conversion Devices. **(Invited)**.

<16:45> Closing remarks

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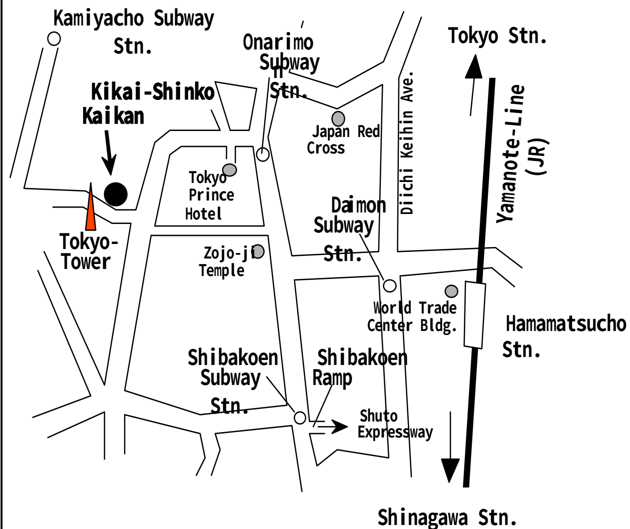

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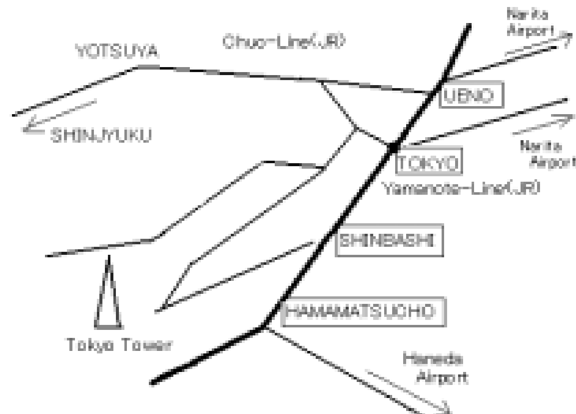

Symposium Chair; Shunri Oda, (*Tokyo Institute of Technology*),
Program Chair; Masaki Yoshimaru (*Oki Electric Industry)*

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ADVANCED PROGRAM

THE 66TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

Kikai Shinko Kaikan, Tokyo, Japan June 24-25, 2004

Organized by:
Electronic Materials Committee,
The Electrochemical Society of Japan.

The 66th Symposium on Semiconductors and Integrated Circuits Technology will be held on June 24-25, 2004 in Tokyo, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced Copper and low-k interconnect technology” and “Novel CMOS devices”.