THE 67TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

ADVANCED PROGRAM

◇ Thursday, **December 16** ◇

<9:25～9:30> Opening remarks by symposium chair

<9:30～10:20>
1. Carbon nanotube vias for future LSI interconnects
M. Nihei[1,2], A. Kawabata[1,2], S. Sato[1,2], D. Kondo[1,2], H. Shioya[1,2], and Y. Awano[1,2],
Fujitsu Laboratories[1], Fujitsu[2]. **(Invited)**

<10:20～10:45>
2. Formation of LSI Interconnection by Bottom-up Electroless Plating of Cu
S.Shingubara, Z.Wang, R.Obata, O.Yaegashi, H.Sakaue, and T.Takahagi, Hiroshima University.

<10:45～11:10>
3. Application of Electro-Chemical Polishing in DI Water to Cu Damascene Wiring Planarization Process
I. Noji, I. Kobata, H. Yasuda, T. Iizumi, M. Kumekawa, Y. Wada, A. Fukunaga, M. Tsujimura, Y. Toma*, T. Suzuki*, and T. Saitoh*,
Ebara, Ebara Research*.

<11:10～12:00>
4. 300mm CMP Technology for Porous Low-k/Cu Process
A. Namiki, S. Tokitoh*, B.U.Yoon*and S.Kondo*,
Novellus Systems Japan, Semiconductor Leading Edge Technologies*.**(Invited)**

<12:00～13:00> Lunch

<13:00～13:50>
5. Pore Structure-control for PECVD-derived SiOCH Film
Y. Hayashi, NEC. **(Invited)**

<13:50～14:15>
6. Characterization of Damage to Porous Low-k Material Caused by Remote Plasma Ashing
O. Inoue, T. Jimbo, K. Katsuyama, and T. Tamaru, Hitachi.

<14:15～14:40>
7. Characterizations of Asing Damage in Low-k Dielectric Films
H. Seki, Y. Otsuka, N. Nagai, H. Hashimoto, M. Shimada* and S. Ogawa*,
Toray Research Center, Semiconductor Leading Edge Technologies*.

<14:40～14:50> Break

<14:50～15:15>
8. Spin-on Dielectric Stack Low-k Integration with EB-Curing Technology for 45nm-node and beyond
H. Nagai, K. Maekawa, M. Iwashita, M. Muramatsu, K. Kubota, K. Hinata, T. Kokubo*, A. Shiota*, M. Hattori*, H. Nagano**, K. Tokushige**, M. Kodera**, K. Mishima**,
TOKYO ELECTRON AT, JSR*, EBARA**.

<15:15～15:40>
9. A New Barrier Metal Structure with ALD-TaN for Highly Reliable Cu Dual Damascene Interconnects
K. Mori, K. Maekawa, and K. Kobayashi, Renesas Technology.

<15:40～16:50>
10. Chip-level Interconnect Scaling and Copper/Low-k Process Integration Technology for 65nm Node and beyond
H. Shibata, Toshiba. **(Invited)**

<17:00～18:30> Banquet

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◇ Friday , **December 17** ◇

<10:20～11:10>
11. Power-aware 65 nm Node CMOS Technology Using Variable Vdd and Back-bias Control with Reliability Consideration for Back-bias Mode
M. Togo, T. Fukai, Y. Nakahara, S. Koyama, M. Makabe, E. Hasegawa, M. Nagase, T. Matsuda, K. Sakamoto, S. Fujiwara, Y. Goto, T. Yamamoto*, T. Mogami*, M.Ikeda, Y. Yamagata, K. Imai, and Y. Nakashiba,
NEC Electronics, NEC*.**(Invited)**

<11:10～11:35>
12. Fully Compatible Integration of Embedded DRAM with 65nm CMOS Technology
K.Yasumoto, Y.Matubara, M.Habu, S.Matsuda, K.Honda, E.Morifuji, T.Yoshida, K.Kokubun, T.Sakurai, T.Suzuki, J.Yoshikawa, E.Takahashi, K.Hiyama, M.Kanda, R.Ishizuka, M.Moriuchi, H.Koga*, K.Ohno*, Y.Fukuzaki*, Y.Sogo*, H.Takahashi*, N.Nagashima*, Y.Okamoto*, S.Yamada and T.Noguchi,
Toshiba, Sony*.

<11:35～12:00>
13. Re-examination of Impact of Intrinsic Dopant Fluctuations on SRAM Static Noise Margin
F. Tachibana, T. Hiramoto, University of Tokyo.

<12:00～13:00> Lunch

<13:00～13:50>
14. High-reliability CMOS technology for 65-nm node and beyond
T. Yamashita, Renesas Technology. **(Invited)**

<13:50～14:40>
15. HfSiON Transistor Technologies for 65nm-node Low-Standby-Power Devices
Y. Tamura, A. Mineji, T. Sasaki, N. Izumi, T. Watanabe, K. Ozaki, F. Ootsuka, M. Yasuhira, T. Hoshi, S. Kume, H. Amai, T. Ida, T. Aoyama, S. Kamiyama, K. Torii, H. Kitajima, and T. Arikado,
Semiconductor Leading Edge Technologies. **(Invited)**

<14:40～14:50> Break

<14:50～15:15>
16. A Novel STI Process from the View Point of Total Strain Process Design for 45nm Node Devices and Beyond
M. Ishibashi, K. Horita, M. Sawada, M. Kitazawa, M. Igarashi, T. Kuroi, T. Eimori, K. Kobayashi, M. Inuishi and Y. Ohji,
Renesas Technology.

<15:15～15:40>
17. Control of Nitrogen depth profile in radical nitrided silicon oxide film.
K. Kawase[1,3] ,H. Umeda[2], M. Inoue[2], S. Tsujikawa[2], Y. Akamatsu[2], T. Suwa[3], M. Higuchi[3], M. Komura[3], A. Teramoto[3] and T. Ohmi[3],
Mitsubishi, Renesas Technology [2], Tohoku Univ[3].

<15:40～16:30>
18. 45nm CMOS Platform Technology (CMOS6)
M. Iwai, Toshiba. **(Invited)**

<16:30> Closing remarks

Kikai-Shinko Kaikan, Japan

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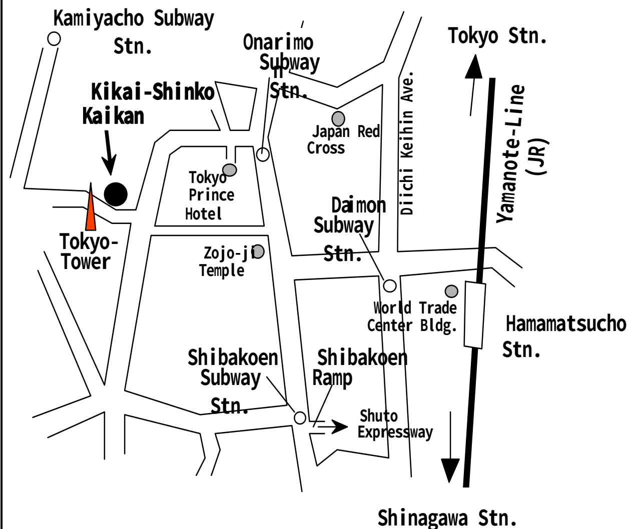

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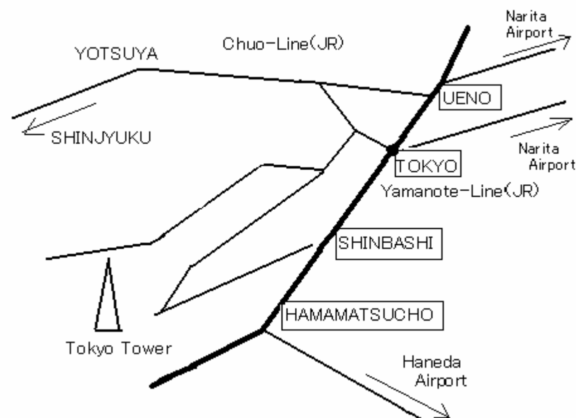

Symposium Chair; Shunri Oda, (*Tokyo Institute of Technology*),
Program Chair; Rempei Nakata (*Toshiba Corporation)*

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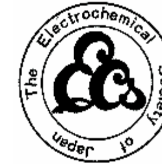

ADVANCED PROGRAM

THE 67TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

Kikai Shinko Kaikan,
Tokyo, Japan
December 16-17, 2004

Organized by:
Electronic Materials Committee,
The Electrochemical Society of Japan.

The 67th Symposium on Semiconductors and Integrated Circuits Technology will be held on December 16-17, 2004 in Tokyo, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced Copper and low-k interconnect technology” and “Device technology for system LSI ”.