THE 68TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

ADVANCED PROGRAM

◇ Thursday, **June 23** ◇

<10:00～10:05> Opening remarks by symposium chair

<10:05～10:55>

1. SOI-CMOS device technology for high speed and low power consumption LSI
   T. Ipposhi, S. Maegawa, and Y. Ohji, Renesas Technology **(Invited)**

<10:55～11:20>

2. Current status of SOI wafer technology and its future prospective
   M. Yoshimi, SOITEC Asia

<11:20～12:10>

3. Sub-10-nm planar-bulk-CMOS device properties
   H. Wakabayashi, T. Ezaki, T. Yamamoto, M. Hane, and T. Mogami, NEC **(Invited)**

<12:10～13:20> Lunch

<13:20～14:10>

4. A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films
   Pidin Sergey, Fujitsu **(Invited)**

<14:10～14:35>

5. Development of high stress SiN films for use with strained silicons technologies
   B. Varadarajan, J. Sims, M. Christensen, K. Ilcisin, K. Shrinivasan, M. Ayoub, V. Dharmadhikari, and M. Xi, Novellus Systems

<14:35～14:45> Break

<14:45～15:10>

6. Chemical dry cleaning technology for reliable 65nm CMOS contact to NiSix
   M. Honda, K. Tsutsumi, H. Harakawa, A. Nomachi, K. Murakami, K. Ooya, T. Kudou, T. Nagamatsu, and H. Ezawa, Toshiba

<15:10～15:35>

7. Charactristics of PVD-HfO2 with poly-Si and fully silicided (FUSI) gates
   S.Hayashi[1], K.Yamamoto[1,2], R.Mitsuhashi[1,2], S.Kubicek[2], S.D.Gendt[2], S.Horii[3], Y.Harada[1], M.Niwa[1,2], and M.Kubota[1], [1]Matsushita Electric Ind., [2]IMEC, [3]Hitachi Kokusai Electric

<15:35～16:00>

8. Changes in structure and composition of the HfSiON film by heat treatment,
   T. Yamamoto, Y. Izumi, T. Miyamoto, J. Tsuji, and H. Hashimoto, Toray Research Center

<16:00～16:50>

9. Development of Fully Silicided Gate technology in Metal /High-k MOSFETs
   T. Nabatame[1], M. Kadoshima[1], A. Ogawa[1], K. Iwamoto[1], M. Takahashi[1], N. Mise[1], S. Migita[2], H. Ota[2], H. Fujiwara[1], H. Satake[1], and A. Toriumi[2,3], [1]MIRAI-ASET, [2]MIRAI-ASRC AIST, [3]The University of Tokyo **(Invited)**

<17:00～18:30> Banquet

*** *** *** *** *** *** *** ***

◇ Friday , **June 24** ◇

<9:50～10:40>

10. Low-k technology for 65 nm node interconnect and beyond
    H. Miyajima[1], M. Hasunuma[1], K. Tabuchi[2], T. Shimayama[2], K. Akiyama[1], T. Hachiya[1], N. Nakamura[1], A. Kajita[1], N. Matsunaga[1], Y. Enomoto[2], R. Kanamura[2], K. Honda[1], H. Yano[1], N. Hayasaka[1], T. Hasegawa*, S. Kadomura*, H. Shibata[1], and T. Yoda[1], [1]Toshiba, [2]Sony **(Invited)**

<10:40～11:05>

11. Structure characterization of SiOC film using solid state NMR spectroscopy
    R. Miyoshi, Y. Miwa, M. Yoshikawa, Toray Research Center

<11:05～11:30>

12. Nano-scale Stress Analysis in Dielectric Films with Cu Interconnects Using Cathodoluminescence Spectroscopy
    S.Kakinuma[1], M.Kodera[2], G.Pezzotti[3], [1]Horiba, [2]Toshiba, [3]Kyoto Institute of Technology

<11:30～11:55>

13. Non-porous low-k fluorocarbon films for 45nm generation formed by very low electron temperature plasma
    K. Miyatani[1], Y. Kobayashi[1], K. Kawamura[1], S. Hosaka[1], T. Matsuoka[1], M. Hirayama[2], A. Teramoto[2], S. Sugawa[2], and T. Ohmi[2], [1]Tokyo Electron, [2]Tohoku University

<11:55～12:20>

14. Novel Ultra Low-k Borazinic Films Prepared by PECVD
    T. Kumada, A. Sasahara, N. Matsumoto, N. Yasuda, H. Nobutoki, T. Toyoshima, and S. Matsuno, Mitsubishi Electric

<12:20～13:20> Lunch

<13:20～14:10>

15. Evaluation of nm-order structures of low-k films by TEM correlated with Cu/low-k processes
    S. Ogawa[1], J. Shimanuki[2], M. Shimada[1], and Y. Inoue[2], [1]Semiconductor Leading Edge Technologies, [2]Nissan ARC **(Invited)**

<14:10～15:00>

16. Electro-chemical mechanical planarization using conductive polishing pad
    S. Kondo[1], S. Tominaga[2], A. Namiki[1], K. Yamada[1], D. Abe[2], K. Fukaya[1], M. Shimada[1], and N. Kobayashi[1], [1]Semiconductor Leading Edge Technologies, [2]Roki Techno **(Invited)**

<15:00～15:25>

17. Development of resist planarization process for Cu/low-k dual damascene
    A. Shigeta, Y. Matsui, G. Minamihaba, Y. Tateyama, K. Takahata, T. Nishioka, H. Yano, N. Hayasaka, Toshiba

<15:25～15:35> Break

<15:35～16:25>

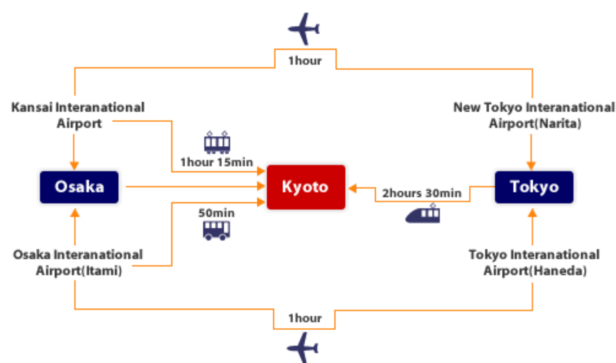
18. Suppression of bimodal stress-induced voiding using high-diffusive dopant from Cu-alloy seed layer
    T. Tonegawa, NEC Electronics **(Invited)**

<16:25～16:50>

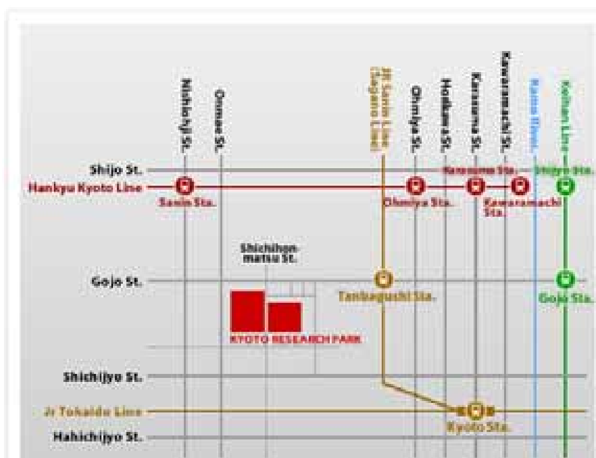
19. Improvement in reliability of Cu dual-damascene interconnects using CuAl alloy seed
    K. Maekawa[1], K. Mori[1] K. Kobayashi[1], M. Yoneda[1], Niranjan Kumar[2], Schubert Chu[2], Samuel Chen[2], Gigi Lai[2], and Daniel L. Diehl[3], [1]Renesas Technology, [2]Applied Materials, [3]Applied Materials Japan

<16:50> Closing remarks

Kyoto Research Park
134, Chudoji Minami-machi, Shimogyo-ku Kyoto
600-8813, Japan
TEL : +81-75-315-8665



Access to Kyoto Research Park, Kyoto
Approx. 75 minutes by JR Airport Express "Haruka" from Kansai International Airport to Kyoto Station
Approx. 5 minutes by JR San'in Honsen (JR Sagano line) train from Kyoto Station to Tambaguchi Station
5 minutes walk from Tambaguchi Station



Symposium Chair: S. Oda *(Tokyo Inst. of Technol.)*
Program Chair: K. Kobayashi *(Tokai University)*
Program Co-Chair: M. Kubota *(Matsushita Electric)*

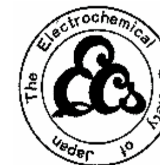
Electronic Materials Committee

Chairperson: S. Oda *(Tokyo Inst. of Technol.)*
Domestic Members:
N. Awaya *(Sharp),*
S. Matsushita *(Sanyo),*
D. Fukushi *(Eudyna Devices),*
I. Sato *(Tokyo Ohka Kogyo),*
T. Hayashi *(ULVAC),*
T. Honma *(Waseda Univ.)*
M. Inoue *(Taiyo Nippon Sanso),*
T. Kaneoka *(Renesas Technology),*
T. Kubo *(Sumitomo Mitsubishi Silicon),*
M. Kubota *(Matsushita Electric),*
T. Masui *(Shin-Etsu Handotai),*
S. Mori *(Nikon),*
R. Nakata *(Toshiba),*
S. Nozawa *(Sony),*
S. Hosaka *(Tokyo Electron Limited),*
O. Okada *(ANELVA),*
S. Samukawa *(Tohoku Univ.)*
S. Shima *(Ebara),*
Y. Suda *(Tokyo Univ. of Agric. And Technol.),*
H. Suzuki *(NEC Electronics),*
Y. Sugiyama *(Fujitsu),*
N. Takaura *(Hitachi),*
K. Taniguchi *(Osaka Univ.),*
M. Yamaguchi *(Kaneka),*
M. Yoshimaru *(STARC),*
H. Inoue *(ASM Japan),*
H. Matsuhashi *(Oki Electric Industry),*
K. Kobayashi *(Tokai Univ.)*
Overseas Member: M.Yoshida *(Samsung)*

Secretariat, Electronic Materials Committee,
The Electrochemical Society of Japan,
Arusu Ichigaya 202,4-8-30, Kudan-minami,
Chiyoda-ku, Tokyo 102-0074, Japan
(Tel.+81-3-3234-4213, Fax.+81-3-3234-3599)

Hotels near Kyoto Research Park

New Miyako Hotel	Tel. +81-75-661-7111
Hotel New Hankyu	Tel. +81-75-343-5300
Hotel Hokke Club Kyoto	Tel. +81-75-361-1251



ADVANCED PROGRAM

THE 68TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

Kyoto Research Park
Kyoto, Japan
June 23-24, 2005

Organized by:
Electronic Materials Committee,
The Electrochemical Society of Japan.

The 68th Symposium on Semiconductors and Integrated Circuits Technology will be held on June 23-24, 2005 in Kyoto, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced CMOS technologies” and “Advanced copper and low-k interconnect technologies”.