# THE 69TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

## ADVANCED PROGRAM

◇ Thursday, **December 15** ◇ 10:00～16:45

<10:00～10:05> Opening remarks by symposium chair

<10:05～10:55>

**1.** Hybrid Low-k/Cu Damascene Process for 45-32nm Technology Node Using Self-Assembled Porous Ultra Low-k Films

S. Chikaki[1], M. Shimoyama[1], R. Yagi[1], T. Yoshino[2], T. Ono[1], A. Ishikawa[1], N. Fujii[1], N. Hata[2] ,T. Nakayama[1], K. Kohmura[1], H. Tanaka[1], Y. Shishida[1], J. Kawahara[1], T. Yamanishi[1], H. Matsuo[1] ,Y. Seino[2], S. Takada[2], N. Kunimi[1] ,Y. Uchida[1], S. Hishiya[1], K. Kinoshita[1], and T. Kikkawa[2,3]

[1]MIRAI(ASET), [2]MIRAI(AIST), [3]Hiroshima Univ. **(Invited)**

<10:55～11:45>

**2.** UV-Cured ULK Materials for Mechanically Reliable Cu/ULK Interconnect

T. Furusawa[1], N. Miura[1], M. Matsumoto[1], K .Goto[1], S. Hashii[2], Y. Fujiwara[1] ,K. Yoshikawa[1], K. Yonekura[1], Y. Asano[1], T. Ichiki[1], N. Kawanabe[1], T. Matsuzawa[1], and M. Matsuura[1]

[1]Renesas, [2]Renesas Semiconductor Engineering **(Invited)**

<11:45～12:45> Lunch

<12:45～13:35>

**3.** Influence of CMP Process on Defects in SiOC Films and TDDB Reliability

Y. Yamada, N. Konishi, J. Noguchi, T. Jimbo, and O. Inoue

Hitachi **(Invited)**

<13:35～14:00>

**4.** The Competitive Reaction between Slurry and Cleaning Solution

A. Ueno[1], S. Uekusa[1], and M. Kodera[2]

[1]Meiji Univ., [2]Toshiba

<14:00～14:25>

**5.** Analysis of MBT Adsorption Layers on Copper Surface by Spectroscopic Ellipsometry

H. Nishizawa[1], O. Sugiura[2], Y. Matsumura[3], and M. Kinoshita[3]

[1]Tokyo Inst. of Tech., [2]Chiba Inst. of Tech., [3]Nitta Haas

<14:25～14:40> Break

<14:40～15:30>

**6.** Electromigration Mass Transport Mechanism of Cu and Al Damascene Interconnects.

T. Usui

Toshiba **(Invited)**

<15:30～15:55>

**7.** Increase of Cu Line Resistance Caused by Pd Activation in Electroless CoWP Plating

X. Wang[1], A. Owatari[1], T. Ishibashi[1], D. Takagi[1], J. Tsujino[1], T. Koba[1], H. Ono[1], N. Chikazawa[1], T. Ishigami[2], S. Kondo[2], and N. Kobayashi[2]

[1]Ebara, [2]Selete

<15:55～16:20>

**8.** Fabrication of the Electroless NiMoB Films as a Diffusion Barrier Layer on the Low-k Substrate

T. Masuda[1], M. Yoshino[1], S. Wakatsuki[1], J. Sasano[1], I. Matsuda[1], Y. Shacham-Diamand[1,2], and T. Osaka[1]

[1]Waseda Univ, [2]Tel-Aviv Univ.

<16:20～16:45>

**9.** Novel Cu Surface Cleaning Technology Using Extremely Low Oxgen Pressure

K. Endo, N. Shirakawa, Y. Yoshida, T. Mino, E. Gofuku, and E. Suzuki

AIST

<17:00～18:30> Banquet and Award Ceremony

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◇ Friday , **December 16** ◇ 10:00～16:50

<10:00～10:50>

**10.** Research and Development on Next-Generation Nonvolatile Memory in ETRI

B.G. Yu, S.M. Yoon, S.O. Ryu, S.Y. Lee, Y.S. Park, K.J. Choi, and N.Y. Lee

ETRI **(Invited)**

**11.** Interface Engineering of Colossal Electro-Resistance Memory

A. Sawa[1], T. Fujii[1,2], M. Kawasaki[1,2], Y. Tokura[1,3]

[1]AIST, [2]Tohoku Univ., [3]Tokyo Univ. **(Invited)**

<11:40～12:45> Lunch

<12:45～13:10>

**12.** Solid Electrolyte Nanometer Switch

N. Banno[1,2], T. Sakamoto[1,2], S. Kaeriyama[1], M. Mizuno[1], H. Kawaura[1,2], T. Hasegawa[3,2], K. Terabe[4,2], M. Aono[3,2]

[1]NEC, [2]JST, [3]NIMS

<13:10～13:35>

**13.** Spin Transfer Torque Magnetization Switching for the next generation MRAMs

K. Ito[1], J. Hayakawa[1,2], H. Takahashi[1,2], S. Ikeda[2], Y.M. Lee[2], R. Sasaki[2], T. Meguro[2], F. Matsukura[2], H. Ohno[2], T. Devolder[3], and C. Chappert[3]

[1]Hitachi, [2]Tohoku. Univ, [3]Universite Paris Sud

<13:35～13:45> Break

<13:45～14:35>

**14.** Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique

T. Tatsumi, M. Terai, K. Takahashi, K. Manabe, T. Hase, T. Ogura, M. Saitoh, T. Iwamoto, and H. Watanabe

NEC **(Invited)**

<14:35～15:00>

**15.** A Comprehensive Study of Ni Fully Silicided (Ni-FUSI) Metal Gates for High-performance CMOS Devices

[1]K. Hosaka, [1]T. Kurahashi, [2]K. Kawamura, [1]T. Aoyama, and [1]K. Suzuki

[1]Fujitsu Lab., [2]Fujitsu.

<15:00～15:25>

**16.** Characterization of Metal-germanide Gate Electrodes Formed by FUGE (Fully Germanided) Process

Y. Tsuchiya, M. Koyama, J. Koga, and A. Nishiyama

Toshiba

<15:25～15:35> Break

<15:35～16:00>

**17.** Strained-Silicon MOSFETs of Low Leakage Current and High Breakdown Voltage for RF/Analog Applications.

N. Sugii[1], M. Kondo[2], M. Miyamoto[1], Y. Hoshino[2], M. Hatori[2], W. Hirasawa[3], Y. Kimura[1], S. Kimura[1], Y. Kondo[2], and I. Yoshida[2]

[1]Hitachi, [2]Renesas, [3]Renesas Eastern Japan Semiconductor.

<16:00～16:50>

**18.** Strained-Si/SiGe/Ge-On-Insulator CMOS Device Technologies.

S. Takagi[1,2]

[1]MIRAI (AIST), [2]Tokyo Univ. **(Invited)**

<16:50> Closing remarks

Kikai-Shinko Kaikan, Japan

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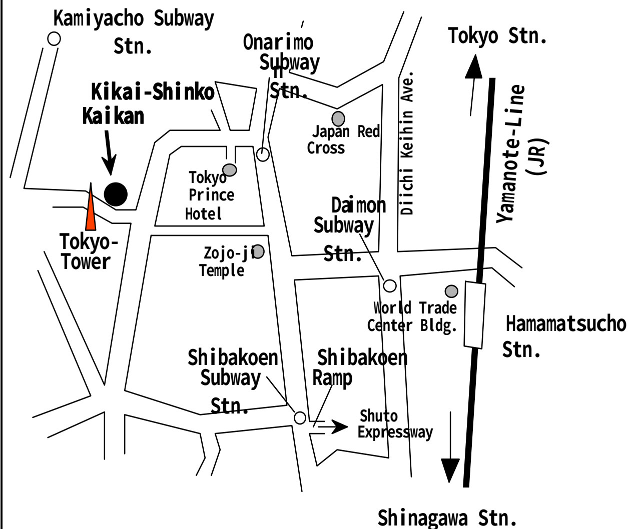


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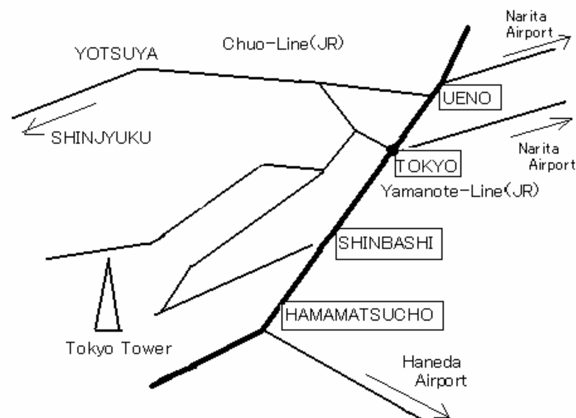


Symposium Chair; Shunri Oda, (*Tokyo Institute of Technology*),
Program Chair; Norikatsu Takaura (*Hitachi*)

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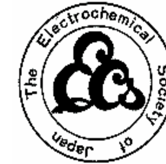


# ADVANCED PROGRAM

# THE 69TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

## Kikai Shinko Kaikan, Tokyo, Japan December 15-16, 2005

**Organized by:**
**Electronic Materials Committee,**
**The Electrochemical Society of Japan.**

The 69th Symposium on Semiconductors and Integrated Circuits Technology will be held on December 15-16, 2005 in Tokyo, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced metal, process, and evaluation technology” and “Novel materials device and memory technology”.