THE 70TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

ADVANCED PROGRAM

◇ Thursday, **July 6** ◇ 10:15～17:00

<10:15～10:20> Opening remarks by symposium chair

<10:20～11:10>
1. Issues for HfSiON Gate Dielectric for Near-future CMOS Devices
M. Koyama, M. Koike, T. Ino, Y. Kamimuta, R. Iijima, and A. Nishiyama
Toshiba **(Invited)**

<11:10～12:00>
2. Nano-scale Evaluations for Degradation Phenomena in Gate Insulators Using Conductive-AFM
S. Zaima[1], A. Seko[1], Y. Watanabe[2], M. Sakashita[1], A. Sakai[1], and M. Ogawa[1]
[1]Nagoya Univ., [2]Toyota Central R&D Lab.**(Invited)**

<12:00～12:25>
3. Vth-tunable CMIS Platform with High-k Gate Dielectrics and Variability Effect for 45nm Node
T. Hayashi, M. Mizutani, M. Inoue, J. Yugami, J. Tsuchimoto, M. Anma, S. Komori, K. Tsukamoto, Y. Tsukamoto, K. Nii, Y. Nishida, H. Sayama, T. Yamashita, H. Oda, T. Eimori, and Y. Ohji
Renesas Tech.

<12:25～13:30> Lunch

<13:30～14:20>
4. Tsukuba Semiconductor Consortium
H. Watanabe
Semiconductor Leading Edge Tech. **(Invited)**

<14:20～14:45>
5. A Study of TiN Metal Gate Electrodes Formed by Divided CVD Technique for pMISFETs
S. Sakashita, T. Kawahara, M. Mizutani, M. Inoue, S. Yamanari, Y. Nishida, K. Mori, N. Murata, K. Honda, J. Tsuchimoto, J. Yugami, and K. Fujiwara
Renesas Tech.

<14:45～15:10>
6. Work Function Control of HfN Gate Electrode
T. Kurahashi, M. Sakamoto, Y. Sakita, and Y. Mishima
Fujitsu Lab.

<15:10～15:20> Break

<15:20～16:10>
7. Plasma Doping
B. Mizuno[1], Y. Sasaki[1], C.G. Jin[1], K. Okashita[1], H. Ito[1], K. Tsutsui[2], and H. Iwai[2]
[1]Ultimate Junction Tech., [2]Tokyo Inst. of Tech. **(Invited)**

<16:10～16:35>
8. New Stress Inducing Technique of Epitaxial Si on Recessed S/D Fabricated in Substrate Strained-Si of <100>-channel on Rotated Wafers
T. Sanuki[1], H. Tanaka[1], K. Oota[2], O. Fujii[1], R. Yamaguchi[1], K. Nakayama[1], Y. Morimasa[1], Y. Takasu[1], J. Idebuchi[1], N. Nishiyama[1], H. Fukui[1], H. Yoshimura[1], K. Matsuo[1], I. Mizushima[1], H. Ito[1], Y. Takegawa[1], M. Saito[2], M. Iwai[1], N. Nagashima[2], and F. Matsuoka[1]
[1]Toshiba, [2]Sony

<16:35～17:00>
9. Analysis of Nano-Scale CMOS Device with TCAD Simulation
R. Tanabe, Y. Ashizawa, and H. Oka
Fujitsu Lab.

<17:15～18:45> Banquet and Award Ceremony

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◇ Friday , **July 7** ◇ 10:20～17:00

<10:20～11:10>
10. Fusion of Semiconductor and MEMS
K. Okumura
Univ. of Tokyo **(Invited)**

<11:10～11:35>
11. Polymer Abrasive Slurry for Cu-CMP
S. Nakamura, K. Shindo, S. Fujii, A. Eto, and T. Ishizuka
Mitsui Chemicals

<11:35～12:25>
12. Development of CMP Process for Cu / Porous Low-k Interconnect
T. Nishioka and H. Yano
Toshiba **(Invited)**

<12:25～13:30> Lunch

<13:30～14:20>
13. Advanced LSI BEOL Module Technology for Ubiquitous Applications
Y. Hayashi
NEC **(Invited)**

<14:20～14:45>
14. Fracture Property Improvements of Porous Low-k Dielectrics
T. Kokubo, M. Sekiguchi, and Y. Takahashi
JSR

<14:45～15:10>
15. Comparison between UV and EB Cure Method for Porous PAr/Porous MSX Hybrid Structure
M. Shimada, K. Fujita, S. Nakao, T. Sakanaka, and H. Miyajima
Toshiba

<15:10～15:20> Break

<15:20～16:10>
16. Self-forming Barrier Process for the 45nm Technology Node using Cu Alloy Metallization
J. Koike
Tohoku Univ. **(Invited)**

<16:10～17:00>
17. Stress Migration Phenomena in Cu/Low-k Interconnects
T. Nakamura[1], T. Suzuki[1], T. Kouno[2], and H. Tuchikawa[1]
[1]Fujitsu Lab., [2]Fujitsu **(Invited)**

<17:00> Closing remarks

Kikai-Shinko Kaikan, Japan

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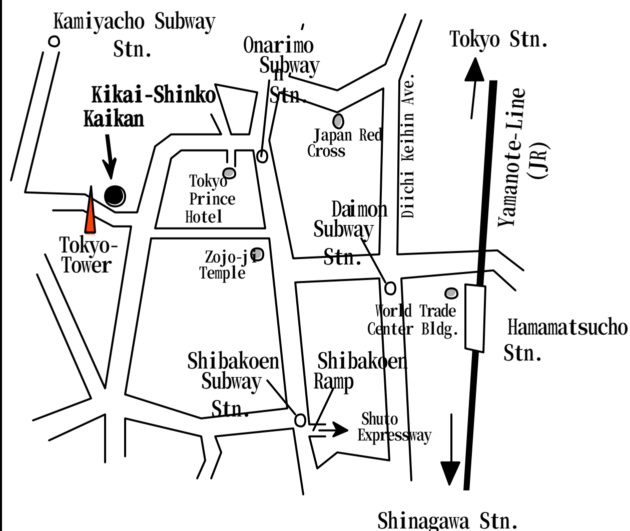

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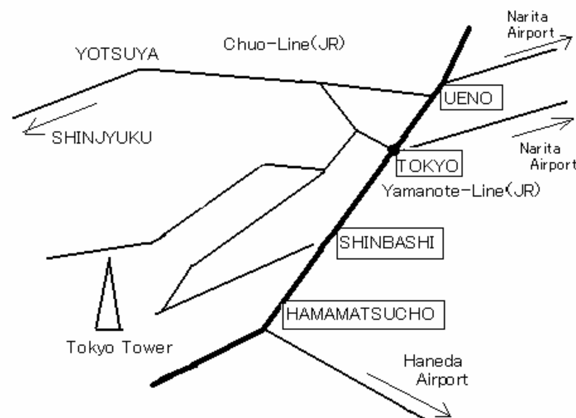

Symposium Chair: Shunri Oda, (*Tokyo Inst. of Technol.*),
Program Chair: Yoshiyuki Suda (*Tokyo Univ. of Agric. and Technol.*)

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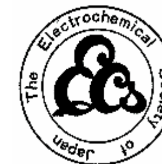

ADVANCED PROGRAM

THE 70TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY

Kikai Shinko Kaikan,
Tokyo, Japan
July 6-7, 2006

Organized by:
Electronic Materials Committee,
The Electrochemical Society of Japan

The 70th Symposium on Semiconductors and Integrated Circuits Technology will be held on July 6-7, 2006 in Tokyo, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced back-end and front-end processes and their related technologies and evaluation technology” and “Novel materials, device and process technologies”.