THE 70TH SYMPOSIUM ON SEMICONDUCTORS AND INTEGRATED CIRCUITS TECHNOLOGY
ADVANCED PROGRAM

Thursday, July 6  □  10:15~17:00
<10:15~10:20> Opening remarks by symposium chair
<10:20~11:10> 1. Issues for HfSiON Gate Dielectric for Near-future CMOS Devices
        M. Koyama, M. Koike, T. Ino, Y. Kamimuta, R. Iijima, and A. Nishiyama
        Toshiba (Invited)
<11:10~12:00> 2. Nano-scale Evaluations for Degradation Phenomena in Gate Insulators Using Conductive-AFM
        S. Zaima1, A. Seko, Y. Watanabe2, M. Sakashita1, A. Sakai1, and M. Ogawa1
        1Nagoya Univ., 2Toyota Central R&D Lab (Invited)
<12:00~12:25> 3. Vth-tunable CMOS Platform with High-k Gate Dielectrics and Variability Effect for 45nm Node
        T. Hayashi, M. Mizutani, M. Inoue, J. Yagami, J. Tsuchimoto, M. Anma, S. Komori, K. Tsukamoto,
        Y. Tsukamoto, K. Nii, Y. Nishida, H. Sayama, T. Yamashita, H. Oda, T. Eimori, and Y. Ohji
        Renesas Tech.
<12:25~13:30> Lunch
<13:30~14:20> 4. Tsukuba Semiconductor Consortium
        Semiconductor Leading Edge Tech. (Invited)
<14:20~14:45> 5. A Study of TiN Metal Gate Electrodes Formed by Divided CVD Technique for pMISFETs
        S. Sakashita, T. Kawahara, M. Mizutani, M. Inoue, S. Yamanari, Y. Nishida, K. Mori,
        N. Murata, K. Honda, J. Tsuchimoto, J. Yugami, and K. Fujiwara
        Renesas Tech.
<14:45~15:10> 6. Work Function Control of HfN Gate Electrode
        T. Kurahashi, M. Sakamoto, Y. Sakita, and Y. Mishima
        Fujitsu Lab.
<15:10~15:20> Break
<15:20~16:10> 7. Plasma Doping
        B. Mizuno1, Y. Sasaki1, C.G. Jin1, K. Okashita1, H. Ito1, K. Tsutsumi2, and H. Iwai2
        1Ultimate Junction Tech., 2Tokyo Inst. of Tech. (Invited)
<16:10~16:35> 8. New Stress Inducing Technique of Epitaxial Si on Recessed S/D Fabricated in Substrate Strained-Si of <100>–channel on Rotated Wafers
        T. Sanuki1, H. Tanaka1, K. Oota2, O. Fujii1, R. Yamaguchi1, K. Nakayama1, Y. Morimasa1,
        Y. Takasu1, J. Idebuchi1, N. Nishiyama1, H. Fukui1, H. Yoshimura1, K. Matsuo1, I. Muzushima1, H. Ito1,
        Y. Takegawa1, M. Saito2, M. Iwai1, N. Nagashima2, and F. Matsuoka1
        1Toshiba, 2Sony
<16:35~17:00> 9. Analysis of Nano-Scale CMOS Device with TCAD Simulation
        R. Tanabe, Y. Ashizawa, and H. Oka
        Fujitsu Lab.
<17:15~18:45> Banquet and Award Ceremony

Friday, July 7  □  10:20~17:00
<10:20~11:10> 10. Fusion of Semiconductor and MEMS
        K. Okumura
        Univ. of Tokyo (Invited)
<11:10~11:35> 11. Polymer Abrasive Slurry for Cu-CMP
        S. Nakamura, K. Shindo, S. Fujii, A. Eto, and T. Ishizuka
        Mitsui Chemicals
        T. Nishioka and H. Yano
        Toshiba (Invited)
<12:25~13:30> Lunch
<13:30~14:20> 13. Advanced LSI BEOL Module Technology for Ubiquitous Applications
        Y. Hayashi
        NEC (Invited)
<14:20~14:45> 14. Fracture Property Improvements of Porous Low-k Dielectrics
        T. Kokubo, M. Sekiguchi, and Y. Takahashi
        JSR
<14:45~15:10> 15. Comparison between UV and EB Cure Method for Porous PA/Par/MSX Hybrid Structure
        M. Shimada, K. Fujita, S. Nakao, T. Sakanaka, and H. Miyajima
        Toshiba
<15:10~15:20> Break
        J. Koike
        Tohoku Univ. (Invited)
<16:10~17:00> 17. Stress Migration Phenomena in Cu/Low-k Interconnects
        T. Nakamura1, T. Suzuki1, T. Kouno2, and H. Tuchikawa1
        1Fujitsu Lab., 2Fujitsu (Invited)
<17:00> Closing remarks
The 70th Symposium on Semiconductors and Integrated Circuits Technology will be held on July 6-7, 2006 in Tokyo, Japan. This symposium brings together scientists and engineers to discuss advances in the field of semiconductors and integrated circuits technology. The official languages of the symposium are Japanese and English. A proceedings volume will be published. Papers are solicited on “Advanced back-end and front-end processes and their related technologies and evaluation technology” and “Novel materials, device and process technologies.”